WE CLAIM:

1. A power management integrated circuit for use in an intelligent electronic device for monitoring at least one parameter of a power system comprising:

an analog front end formed as part of said power management integrated circuit operative to receive and at least one of amplify, attenuate and filter analog signals representative of at least one of voltage and current in a power system to produce modified analog signals;

at least one analog to digital converter formed as part of said power management integrated circuit coupled with said analog front end, wherein said at least one analog to digital converter is operative to produce digital signals representative of said modified analog signals;

first logic formed as part of said power management integrated circuit coupled with said analog to digital converter, operative to receive said digital signals and produce at least one power parameter; said logic comprising at least one processor core;

at least one random access memory formed as part of said power management integrated circuit coupled with said first logic and operative to store said at least one power parameter;

wherein said first logic is operative to implement at least one setpoint to detect when said at least one power parameter is outside a determined range; and

at least one digital output formed as part of said power management integrated circuit coupled with said first logic, wherein said digital output is useable to control a switching circuit outside said power management integrated circuit.

2. The power management integrated circuit of claim 1 wherein said switching circuit is operative to control the application of power from said power system.

3. The power management integrated circuit of claim 2 wherein said switching circuit comprises at least one of a circuit breaker, a relay and a contactor.

4. The power management integrated circuit of claim 3 wherein said at least one power parameter comprises at least one of rms current, rms voltage, watts, power factor, kVA, kVAR, frequency, harmonic distortion, and energy.

5. The power management integrated circuit of claim 1 wherein said at least one power parameter comprises at least one of rms current, rms voltage, watts, power factor, kVA, kVAR, frequency, harmonic distortion, and energy.

6. The power management integrated circuit of claim 1 further comprising:

second logic formed as part of said power management integrated circuit, coupled with said first logic and operative to process at least one incoming fieldbus packet and generate at least one outgoing fieldbus packet encapsulating said at least one power parameter;

at least one communications interface formed as part of said power management integrated circuit coupled with said second logic, said at least one communications interface operative to receive

said at least one incoming fieldbus packet from outside said power management integrated circuit and transmit said at least one outgoing fieldbus packet out of said power management integrated circuit.

7. The power management integrated circuit of claim 6 wherein said at least one incoming fieldbus packet contains a cyclic redundancy check.

8. The power management integrated circuit of claim 6 wherein said at least one incoming fieldbus packet contains a unit ID indicative of an intended destination of said incoming fieldbus packet.

9. The power management integrated circuit of claim 1 further comprising:

second logic formed as part of said power management integrated circuit, coupled with said first logic and operative to process at least one incoming TCP/IP packet and generate at least one outgoing TCP/IP packet encapsulating said at least one power parameter;

at least one communications interface formed as part of said power management integrated circuit coupled with said second logic, said at least one communications interface operative to receive said at least one incoming TCP/IP packet from outside said power management integrated circuit and transmit said at least one outgoing TCP/IP packet out of said power management integrated circuit.

10. The power management integrated circuit of claim 1 further comprising:

a phase lock loop clock circuit formed as part of said power management integrated circuit operative to provide a variable clock signal to said first logic.

11. The power management integrated circuit of claim 1 wherein said at least one random access memory comprises:

a volatile section operative to provide temporary storage during operation of said first logic; and

a non-volatile section operative to contain configuration information for said power management integrated circuit.

12. The power management integrated circuit of claim 1 further comprising a control circuit formed as part of said power management integrated circuit coupled with said first logic, said control circuit operative to control a power supply that supplies operating power to said power management integrated circuit.

13. The power management integrated circuit of claim 1 wherein said at least one power parameter comprises a sample of at least one of a voltage waveform, a current waveform and a power waveform.

14. The power management integrated circuit of claim 1 further comprising a control circuit formed as part of said power management integrated circuit, coupled with said analog front end and operative to control a power supply which supplies operating power to said power management integrated circuit.

15. The power management integrated circuit of claim 14 wherein said control circuit is operative to apply a PWM signal to said power supply.

16. The power management integrated circuit of claim 1 wherein said at least one random access memory comprises magnetic random access memory.

17. The power management integrated circuit of claim 1 further comprising a supervisor circuit formed as part of said power management integrated circuit, operative to monitor a voltage level from a supply of power outside said power management integrated circuit and provide a signal to said power management integrated circuit when a voltage of said supply of power falls outside a bound.

18. The power management integrated circuit of claim 1 wherein said first logic is operative to compensate for distortion in at least one of said analog front end, said at least one analog to digital converter and an external transformer capable of being coupled with said power management integrated circuit.

19. The power management integrated circuit of claim 1 further comprising a display driver formed as part of said power management integrated circuit, coupled with said first logic and operative to drive a display external to said power management integrated circuit.

20. The power management integrated circuit of claim 19 wherein said display is a graphical display.

21. The power management integrated circuit of claim 1 further comprising circuitry formed as part of said power management integrated circuit operative to convert at least one of said analog signals to a digital signal indicative of the fundamental frequency of said at least one of said analog signals.

22. The power management integrated circuit of claim 1 further comprising a JTAG interface coupled with said first logic.

23. The power management integrated circuit of claim 1 wherein said at least one power parameter comprises an indication of a power quality event.

24. The power management integrated circuit of claim 1 wherein said determined range comprises an I^2T relationship.

25. An intelligent electronic device for monitoring at least one parameter of a power system comprising:

A power supply operative to couple with a power system and provide operating power for said intelligent electronic device;

interface circuitry coupled with said power supply and operative to be coupled with at least one of a voltage and a current signal from a power system; and

the power management integrated circuit of claim 1 coupled with said power supply and said interface circuitry.

26. A power monitoring system comprising:

a first intelligent electronic device comprising the intelligent electronic device of claim 25;

a second intelligent electronic device coupled with said first intelligent electronic device, wherein said second intelligent electronic device is operative to receive and store said at least one power parameter in a second random access memory included in said second intelligent electronic device;

wherein said second intelligent electronic device is operative to implement at least one second setpoint to detect when said at least one power parameter is outside a second determined range; and

at least one second digital output controllable with said second intelligent electronic device, wherein said second digital output is useable to control a second switching circuit outside said second intelligent electronic device.

27. The power monitoring system of claim 26 wherein at least one of said first intelligent electronic device and said second intelligent electronic device comprises a protective relay.

28. The power monitoring system of claim 26 wherein said second switching circuit is operative to control the application of power from said power system.

29. The intelligent electronic device of claim 25 further comprising:

second logic formed as part of said power management integrated circuit, coupled with said first logic and operative to process at least one incoming fieldbus packet and generate at least one outgoing fieldbus packet encapsulating said at least one power parameter; and

at least one communications interface formed as part of said power management integrated circuit coupled with said second logic, said at least one communications interface operative to receive said at least one incoming fieldbus packet from outside said power management integrated circuit and transmit said at least one outgoing fieldbus packet out of said power management integrated circuit.

30. The intelligent electronic device of claim 25 further comprising:

second logic formed as part of said power management integrated circuit, coupled with said first logic and operative to process at least one incoming TCP/IP packet and generate at least one outgoing TCP/IP packet encapsulating said at least one power parameter; and

at least one communications interface formed as part of said power management integrated circuit coupled with said second logic, said at least one communications interface operative to receive said at least one incoming TCP/IP packet from outside said power management integrated circuit and transmit said at least one outgoing TCP/IP packet out of said power management integrated circuit.

31. The intelligent electronic device of claim 25 wherein said at least one random access memory comprises:

a volatile section operative to provide temporary storage during operation of said first logic; and

a non-volatile section operative to contain configuration information for said power management integrated circuit.

32. The intelligent electronic device of claim 25 further comprising a control circuit formed as part of said power management integrated circuit coupled with said first logic, said control circuit operative to control said power supply.

33. The intelligent electronic device of claim 25 further comprising:

a display coupled with said power management integrated circuit;

wherein said power management integrated circuit further comprises a display driver coupled with said first logic and operative to drive said display.

34 A power management integrated circuit for use in an intelligent electronic device for monitoring at least one parameter of a power system comprising:

an analog front end formed as part of said power management integrated circuit operative to receive and at least one of amplify, attenuate and filter analog signals to produce modified analog signals, said modified analog signals representative of at least one of voltage and current in a power system;

at least one analog to digital converter formed as part of said power management integrated circuit coupled with said analog front end, wherein said at least one analog to digital converter is operative to produce digital signals representative of said modified analog signals;

first logic formed as part of said power management integrated circuit coupled with said at least one analog to digital converter, operative to receive said digital signals, operative to interface to a source of time and associate a timestamp with said digital signals to produce timestamped digital signals; said first logic comprising at least one processor core;

at least one random access memory coupled with said first logic and operative to store said timestamped digital signals; and

a communications interface coupled with said first logic, wherein said communications interface is operative to transmit said timestamped digital signals for receipt by devices external to said power management integrated circuit.

35. The power management integrated circuit of claim 34 wherein said source of time comprises a GPS receiver.

36. The power management integrated circuit of claim 34 wherein said communication interface is operative to receive communication packets transmitted to said power management integrated circuit and said source of time comprises a communications packet.

37. The power management integrated circuit of claim 34 wherein said source of time comprises a clock.

38. The power management integrated circuit of claim 34 wherein said first logic is operative to detect a power quality event in said at least one of voltage and current.

39. The power management integrated circuit of claim 34 further comprising a JTAG interface coupled with said first logic.

40. The power management integrated circuit of claim 34 wherein said first logic is operative to compensate for distortion in at least one of said analog front end, said at least one analog to digital converter and an external transformer capable of being coupled with said power management integrated circuit.

41. The power management integrated circuit of claim 34 wherein said at least one random access memory comprises magnetic random access memory.

42. The power management integrated circuit of claim 34 further comprising a control circuit formed as part of said power management integrated circuit coupled with said analog front end, said control circuit operative to control a power supply that supplies operating power to said power management integrated circuit.

43. The power management integrated circuit of claim 42 wherein said control circuit is operative to control said power supply with a pulse width modulated signal.

44. The power management integrated circuit of claim 34 further comprising:

second logic formed as part of said power management integrated circuit coupled with said first logic and operative to process at least one incoming TCP/IP packet and generate at least one outgoing TCP/IP packet encapsulating said timestamped digital signals; and

wherein said communications interface is coupled with said second logic and is operative to receive said at least one incoming TCP/IP packet from outside said power management integrated circuit and transmit said at least one outgoing TCP/IP packet out of said power management integrated circuit.

45. The power management integrated circuit of claim 34 further comprising:

a phase lock loop clock circuit operative to provide a variable clock signal to said first logic.

46. A power monitoring system comprising:

A first intelligent electronic device incorporating the power management integrated circuit of claim 34; and

A second intelligent electronic device coupled with said first intelligent electronic device, said second intelligent electronic device operative to receive said digital signals via a communications pathway from said first intelligent electronic device and further operative to compute at least one power parameter as a function of said digital signals.

47. The power monitoring system of claim 46 wherein said source of time comprises a GPS receiver.

48. The power monitoring system of claim 46 wherein said communication interface is operative to receive communication packets transmitted to said power management integrated circuit and said source of time comprises a communications packet.

49. The power monitoring system of claim 46 wherein said source of time comprises a clock.

50. The power monitoring system of claim 46 wherein said first logic is operative to detect a power quality event in said modified analog signals.

51. The power monitoring system of claim 46 wherein said power management integrated circuit further comprises a JTAG interface coupled with said first logic.

52. The power monitoring system of claim 46 further comprising a power supply to supply operating power to said power management integrated circuit wherein said power management integrated circuit further comprises a control circuit coupled with said analog front end, said control circuit operative to control said power supply as a function of at least one of said operating power and said modified analog signals.

53. The power monitoring system of claim 52 wherein said control circuit is operative to control said power supply with a pulse width modulated signal.

54. The power monitoring system of claim 46 wherein said communications interface is operative to receive at least one incoming TCP/IP packet from outside said power management integrated circuit and said first logic is operative to process said at least one incoming TCP/IP packet and generate at least one outgoing TCP/IP packet encapsulating said timestamped digital signals.

55. The power monitoring system of claim 46 wherein

said at least one random access memory is a first random access memory operative to store data; and

said second intelligent electronic device comprises a second random access memory operative to store data;

wherein said first and second intelligent electronic devices are operative to communicate in order to keep said data stored in said first and second random access memories equivalent.

56. The power monitoring system of claim 55 wherein said second intelligent electronic device comprises a protective relay.

57. A power management integrated circuit for use in an intelligent electronic device for monitoring at least one parameter of a power system comprising:

a digital interface formed as part of said power management integrated circuit operative to receive digital signals representative of at least one of voltage and current in a power system;

first logic formed as part of said power management integrated circuit coupled with said digital interface operative to receive said digital signals and produce at least one power parameter; said logic further comprising at least one processor core;

at least one random access memory formed as part of said power management integrated circuit coupled with said first logic and operative to store said at least one power parameter;

wherein said first logic is operative to implement at least one setpoint to detect when said at least one power parameter is outside a determined range; and

at least one digital output formed as part of said power management integrated circuit coupled with said first logic, wherein said digital output is useable to control a switching circuit outside said power management integrated circuit.

58. The power management integrated circuit of claim 57 wherein said switching circuit is operative to control the application of power from said power system.

59. The power management integrated circuit of claim 58 wherein said switching circuit comprises at least one of a circuit breaker, a relay and a contactor.

60. The power management integrated circuit of claim 59 wherein said at least one power parameter comprises at least one of rms current, rms voltage, watts, power factor, kVA, kVAR, frequency, harmonic distortion, and energy.

61. The power management integrated circuit of claim 57 wherein said at least one power parameter comprises at least one of rms current, rms voltage, watts, power factor, kVA, kVAR, frequency, harmonic distortion, and energy.

62. The power management integrated circuit of claim 57 further comprising:

second logic formed as part of said power management integrated circuit coupled with said first logic and operative to process at least one incoming fieldbus packet and generate at least one outgoing fieldbus packet encapsulating said at least one power parameter;

at least one communications interface formed as part of said power management integrated circuit coupled with said second logic and operative to receive said at least one incoming fieldbus packet from outside said power management integrated circuit and transmit said outgoing fieldbus packet out of said power management integrated circuit.

63. The power management integrated circuit of claim 62 wherein said at least one incoming fieldbus packet contains a cyclic redundancy check.

64. The power management integrated circuit of claim 62 wherein said at least one incoming fieldbus packet contains a unit ID indicative of an intended destination of said at least one incoming fieldbus packet.

65. The power management integrated circuit of claim 57 further comprising:

second logic formed as part of said power management integrated circuit coupled with said first logic and operative to process at least one incoming TCP/IP packet and generate at least one outgoing TCP/IP packet encapsulating said at least one power parameter;

at least one communications interface formed as part of said power management integrated circuit coupled with said second logic, said at least one communications interface operative to receive said at least one incoming TCP/IP packet from outside said power management integrated circuit and transmit said at least one outgoing TCP/IP packet out of said power management integrated circuit.

66. The power management integrated circuit of claim 57 further comprising:

a phase lock loop clock circuit formed as part of said power management integrated circuit operative to provide a variable clock signal to said first logic.

67. The power management integrated circuit of claim 57 wherein said at least one random access memory comprises:

a volatile section operative to provide temporary storage during operation of at least one of said first and second logic; and

a non-volatile section operative to contain configuration information for said power management integrated circuit.

68. The power management integrated circuit of claim 57 wherein said at least one power parameter comprises a sample of at least one of a voltage waveform, a current waveform and a power waveform.

69. The power management integrated circuit of claim 57 further comprising a control circuit formed as part of said power management integrated circuit coupled with said first logic and operative to control a power supply which supplies operating power to said power management integrated circuit.

70. The power management integrated circuit of claim 69 wherein said control circuit is operative to apply a PWM signal to said power supply.

71. The power management integrated circuit of claim 57 wherein said at least one random access memory comprises magnetic random access memory.

72. The power management integrated circuit of claim 57 further comprising a supervisor circuit formed as part of said power management integrated circuit operative to monitor a voltage level from a supply of power outside said power management integrated circuit and provide a signal to said power management integrated circuit when a voltage of said supply of power falls outside a bound.

73. The power management integrated circuit of claim 57 wherein said first logic is operative to compensate for distortion in an external transformer capable of being coupled with said power management integrated circuit.

74. The power management integrated circuit of claim 57 further comprising a display driver formed as part of said power management integrated circuit coupled with said first logic and operative to drive a display external to said power management integrated circuit.

75. The power management integrated circuit of claim 74 wherein said display is a graphical display.

76. The power management integrated circuit of claim 57 further comprising a JTAG interface coupled with said first logic.

77. The power management integrated circuit of claim 57 wherein said at least one power parameter includes an indication of a power quality event.

78. The power management integrated circuit of claim 57 wherein said determined range comprises an I^2T relationship.

79. The power management integrated circuit of claim 65 wherein said communications interface comprises at least one of a DSL interface, a cable modem interface, a serial interface and a telephone modem interface.

80. An intelligent electronic device for monitoring at least one parameter of a power system comprising:

a power supply operative to couple with a source of power and provide operating power for said intelligent electronic device; and

the power management integrated circuit of claim 57 coupled with said power supply and said interface circuitry.

81. A power monitoring system comprising:

a first intelligent electronic device comprising the intelligent electronic device of claim 80;

a second intelligent electronic device coupled with said first intelligent electronic device, wherein said second intelligent electronic device is operative to receive and store said at least one power parameter in a second random access memory included in said second intelligent electronic device;

wherein said second intelligent electronic device is operative to implement at least one second setpoint to detect when said at least one power parameter is outside a second determined range; and

at least one second digital output controllable with said second intelligent electronic device, wherein said second digital output is useable to control a second switching circuit outside said second intelligent electronic device.

82. The system of claim 81 wherein at least one of said first intelligent electronic device and said second intelligent electronic device comprise a protective relay.

83. The intelligent electronic device of claim 80 wherein said switching circuit is operative to control the application of power from said power system.

84. The intelligent electronic device of claim 80 further comprising:

second logic formed as part of said power management integrated circuit, coupled with said first logic and operative to process at least one incoming fieldbus packet and generate at least one outgoing fieldbus packet encapsulating said at least one power parameter;

at least one communications interface formed as part of said power management integrated circuit coupled with said second logic, said at least one communications interface operative to receive said at least one incoming fieldbus packet from outside said power management integrated circuit and transmit said at least one outgoing fieldbus packet out of said power management integrated circuit.

85. The intelligent electronic device of claim 80 further comprising:

second logic formed as part of said power management integrated circuit, coupled with said first logic and operative to process at least one incoming TCP/IP packet and generate at least one outgoing TCP/IP packet encapsulating said at least one power parameter; and

at least one communications interface formed as part of said power management integrated circuit coupled with said second logic, said at least one communications interface operative to receive said at least one incoming TCP/IP packet from outside said power management integrated circuit and transmit said at least one outgoing TCP/IP packet out of said power management integrated circuit.

86. The intelligent electronic device of claim 80 wherein said at least one random access memory comprises:

a volatile section operative to provide temporary storage during operation of said first logic; and

a non-volatile section operative to contain configuration information for said power management integrated circuit.

87. The intelligent electronic device of claim 80 further comprising a control circuit formed as part of said power management integrated circuit coupled with said first logic, said control circuit operative to control said power supply.

88. The intelligent electronic device of claim 80 further comprising:

a display coupled with said power management integrated circuit;

wherein said power management integrated circuit further comprises a display driver coupled with said first logic and operative to drive said display.

89. A power management integrated circuit for use in an intelligent electronic device for monitoring at least one parameter of a power system comprising:

an interface formed as part of said power management integrated circuit operative to receive signals epresentative of at least one of voltage and current in a power system and produce modified signals indicative of said signals;

first logic formed as part of said power management integrated circuit operative to receive said modified signals and produce at least one power parameter;

a communications interface formed as part of said power management integrated circuit coupled with said first logic and operative to transmit said power parameter out of said power management integrated circuit; and

a control circuit formed as part of said power management integrated circuit coupled with said first logic and operative to control a power supply which supplies operating power to said power management integrated circuit.

90. The power management integrated circuit of claim 89 wherein said control circuit is operative to apply a PWM signal to said power supply.